FABRICATION METHOD FOR HETEROJUNCTION BIPOLAR TRANSISTOR

ABSTRACT OF THE INVENTION

A fabrication method for heterojunction bipolar transistor is disclosed. The method uses ISSG oxide instead of conventional PECVD oxide so that the base/emitter interface damage can be reduced. Moreover, the invention replaces the conventional emitter-window/space mask with an emitter-window reverse-tone mask/line mask to minimize the critical dimension of emitter window. Furthermore, the invention also utilizes a two-steps extrinsic base implantation to form two extrinsic bases with different dopant concentrations so that the base resistance can be reduced.